Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A CMOS circuit comprising:

a first gate reference voltage;

a first bias circuit source; and

a device for adjusting a current from the first bias current source to a first circuit to reduce the variation of the first circuit as a function of process, voltage and temperature, the device including:

a first transistor having a gate, a first node and a second node, ~~having its~~ the gate of the first transistor being coupled to the first gate reference voltage, ~~the device~~ the first node of the first transistor being coupled ~~in series with~~ to the first bias current source ~~and having a gate size and structure to enhance its sensitivity to process, voltage and temperature variations~~, the first transistor for generating a current sensitive to process, voltage and temperature variations;

a second transistor coupled to the first circuit and having a gate, a first node and a second node, the gate and the first node of the second transistor being coupled to the first node of the first transistor and the first bias current source, the second transistor for adjusting a current proportional to the difference between the current generated by the first bias current source and the current from the first transistor thereby compensating the current of the first bias current source for the ~~same~~ process, voltage and temperature variations.

2.-10. (Cancelled)

11. (Withdrawn) A physical layer segment including:

a transmitter having:

an output coupled to a communication medium,

and a first pseudo-random bit-stream generator coupled to said output,

a receiver having:

an input coupled to a communication medium,

a second pseudo-random bit-stream generator

and a comparator coupled to said input and said second pseudo-random bit-stream generator;

12. (Withdrawn) A physical layer segment according to claim 11 wherein the receiver includes, a bit error rate counter coupled to said comparator.

13. (Withdrawn) A method of establishing data integrity comprising:

receiving a series of vectors,

generating the first of a series of pseudo-random vectors,

comparing said received and said first generated vector,

and after a positive comparison,

generating the remainder of said series and comparing these with subsequently received vectors.

14. (Withdrawn) A multiplexing circuit having:

a test data input;

a plurality of non-test data inputs;

an output;

a test mode selection input;

a selection input;

a plurality of intermediate signal lines;

an enabling means, coupled to said test mode selection input, for determining which of said plurality of non-test data inputs or said test data input is coupled said plurality of intermediate signal lines;

and a selection means, coupled to said selection input, for determining which of said intermediate signal lines is coupled to said output.

15. (Withdrawn) The multiplexing circuit according to claim 14 wherein a clock signal is coupled to the selection input.

16. (Withdrawn) The multiplexing circuit according to claim 15 wherein the output is coupled to a double data rate data signal.

17. (Withdrawn) The multiplexing circuit according to claim 14 wherein a JTAG test output data is coupled to the test data input and a JTAG test mode enable signal is coupled to the test mode selection input.

18. (Withdrawn) A physical layer segment including a delay line generator comprising:

A first bias generator,

And a second bias generator having:

a positive reference,

a negative reference,

a first bandgap reference,

and a second bandgap reference,

A voltage control input,

A delay line output,

A first MOSFET having a first doping,

Conductively coupling said first reference to said delay line output,

And coupled at its gate to said voltage control input,

A second MOSFET having a first doping,

Conductively coupling said first reference to said delay line output,

And coupled at its gate to said first bandgap reference,

A third MOSFET having a complementary doping to said first doping,

Conductively coupling said second reference to said delay line output,

And coupled at its gate to said second bandgap reference,

And a fourth MOSFET having a complementary doping to said first doping,

Conductively coupling said second reference to said delay line output,

And coupled at its gate to said delay line output.

19. (New) A CMOS circuit as claimed in Claim 1, wherein the structure of the gate of the first transistor includes a plurality of stripes.

20. (New) A CMOS circuit as claimed in Claim 1, wherein the first transistor and the second transistor are NMOS transistors, the first node of the first transistor being a drain, the first node of the second transistor being a drain.

21. (New) A CMOS circuit as claimed in Claim 1, wherein the first circuit includes at least one of a delay cell, a delay lock loop (DLL), a phase lock loop (PLL), a charge pump, an Operational Amplifier, and an Input/Output pad.